Design and Implementation of a 6th Order SC Butterworth Lowpass Filter
ELE 539 Design Project

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Abstract

This report describes the design and implementation of a switched-capacitor filter, using the methods of analog filter design and continuous to discrete time pole transformation to obtain a z-domain equivalent system, which can be implemented by using general SC biquad circuits. The requirements for this filter are:

Filter Type:	Butterworth Lowpass
Filter Order:	6
Cut-off Frequency:	20kHz
Sampling Frequency:	400kHz
Topology:	General SC biquads
Semiconductor Process:	AMI 1.2μm

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Chapter 1

Introduction

Despite the rapidly growing trend of processing all kinds of signals digitally there will always be the need of hardware to interface the analog and the digital world. With the introduction of the switched-capacitor (SC) technique in the late 1970's the implementation of analog and digital subsystems on the same integrated circuit using the same technology became feasible.

Before an analog signal can be sampled and quantized it has to be lowpass filtered in order to avoid aliasing. If realized using only analog circuitry these generally high-order filters become very complex and expensive. To be able to reduce the analog lowpass filter to a first order network the signal would have to be oversampled many times. Additional filtering before quantizing the signal could then be done in the discrete-time domain.

This leads to the utilization of a SC lowpass filter which is a hybrid between a digital and an analog network: It has the time-discrete nature of digital circuits, but at the same time it preserves the continuous signal level. If built correctly, the input stage of an SC lowpass filter can fulfill the task of a Sample/Hold circuit.

In Chapter 2 we show the design of a 6th order Butterworth lowpass filter according to given specifications. Even though the SC filter is a discrete-time circuit the placement of the Butterworth poles can be done much more easily in the continuous-time domain. The chapter then describes the transformation of the continuous-time Butterworth poles to the discrete-time domain using a matched z-transform. In addition we show the derivation of the z-domain equivalent transfer function for the desired Butterworth filter.

Chapter 3 introduces a SC topology that realizes the discrete-time transfer function derived in Chapter 2 and describes the calculation of its circuit coefficients. After verifying the performance of the filter by means of a time domain based simulation we show the determination of the capacitor sizes needed to implement the circuit.

In Chapter 4 we describe the implementation of the design in VLSI technology. Besides presenting the development and combination of modular building blocks used for the implementation we show an effective way of laying out the circuit in compliance with certain requirements such as area, noise insensitivity and speed.

Finally, Chapter 5 concludes this report by pointing out the steps that would follow the work accomplished within the framework of this design project.

Chapter 2

Filter Design

2.1 The Continuous Time Lowpass Filter

The general s-domain transfer function of an nth order lowpass can be written as:

$$H(S) = \frac{H_0}{\sum_{i=0}^{n} c_i S_i^i} \tag{2.1}$$

where,

$$c_0 = 1 \quad \text{and} \quad S = \frac{s}{\omega_p}$$

The coefficients $c_1, c_2, \ldots c_n$ of the denominator polynomial in (2.1) are all real and positive. The order of the lowpass filter is equal to the highest power of S. For the realization of the filter it is beneficial to factorize the denominator polynomial. By allowing complex poles a decomposition into linear factors is no longer possible, but a product of quadratic terms can be obtained:

$$H(S) = \frac{H_0}{\prod_{i=1}^{m} (1 + a_i S + b_i S^2)} \tag{2.2}$$

a_i and b_i are positive real coefficients. For an odd order the coefficient b_1 is equal to zero.

The frequency response of such a filter can be optimized to meet certain requirements, which leads to specific values for the coefficients a_i and b_i depending on the desired lowpass filter type [1].

The transfer function for each second order section can be written as:

$$H_i(s) = \frac{H_{i_0}}{1 + a_i \frac{s}{\omega_p} + b_i \frac{s^2}{\omega_p^2}} \tag{2.3}$$

where,

$$a_i = \frac{\omega_p}{\omega_{p_i} Q_i} \quad \text{and} \quad b_i = \frac{\omega_p^2}{\omega_{p_i}^2}$$

H_{i_0} is the DC gain and ω_{p_i} is the cut-off frequency of the corresponding lowpass biquad. Q_i is its filter quality factor and ω_p denotes the cut-off frequency of the entire lowpass filter.

2.2 s-Domain Butterworth Lowpass Biquad

For the special case of a Butterworth lowpass filter the individual biquads only differ in their quality factors Q_i. They all have the same cut-off frequency which is equal to the cut-off frequency ω_p of the entire filter, i.e. $\forall i : \; a_i = \frac{1}{Q_i} \; , \; b_i = 1$. Therefore, the transfer function of an individual Butterworth biquad with unity gain can be written as:

$$H_i(s) = \frac{1}{1 + s\frac{1}{\omega_p Q_i} + s^2 \frac{1}{\omega_p^2}} \tag{2.4}$$

The correct quality factors Q_i can be obtained from tables [1]. For our case, the 6th order Butterworth lowpass filter, three second order sections are required. The corresponding quality factors listed in Table 2.1.

i	Q_i
1	0.5176
2	0.7071
3	1.9320

Table 2.1: Q_i for a 6th order Butterworth lowpass filter.

2.3 From Continuous to Discrete ...

Since a switched capacitor filter is a discrete time circuit, the poles of the continuous time biquad have to be transformed from the s-domain to the z-domain. The poles of $H_i(s)$ are the roots of the denominator polynomial of (2.4):

$$s_{1/2} = -\frac{\omega_p \left(1 \pm \sqrt{1 - 4Q_i^2}\right)}{2Q_i} \tag{2.5}$$

These poles can be transformed to the discrete time domain by using the matched z-transform

$$z_i = e^{s_i T} \tag{2.6}$$

where T denotes the sampling interval. By plugging (2.5) into (2.6) we obtain

$$z_{s_{1/2}} = e^{-\frac{\omega_p T \left(1 \pm \sqrt{1-4Q_i^2}\right)}{2Q_i}} \tag{2.7}$$

as desired pole locations in the z-domain. Figure 2.1 shows the original poles

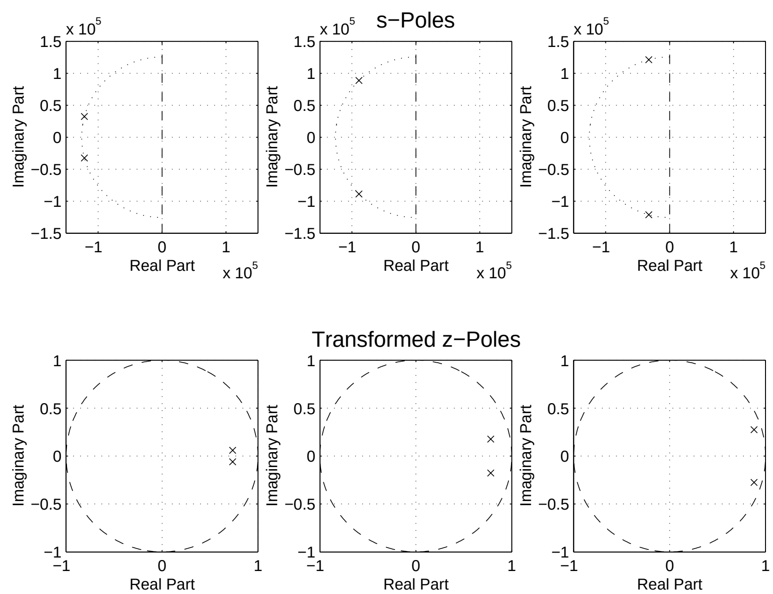

Figure 2.1: s-poles and transformed z-poles.

in the s-domain and the to the z-domain transformed poles of our 6th order Butterworth lowpass filter for a sampling frequency of f_s=400kHz. Note, that all the s-poles have the same magnitude (indicated by the dotted circle), and that their phase angles are equally spaced along the interval $[\frac{\pi}{2}, \frac{3\pi}{2}]$. This is the special property of all Butterworth polynomials.

2.4 Discrete Time Lowpass Biquad

The z-domain transfer function of a lowpass biquad can be written as:

$$H(z) = \frac{a_1}{z^2 + b_1 z + b_0} \tag{2.8}$$

In order to obtain a discrete time Butterworth biquad the poles of (2.8) have to be equal to the desired poles in (2.7). This is one requirement for $H(z)$. The poles of (2.8) are

$$z_{1/2} = -\frac{b_1\left(1 \pm \sqrt{1 - 4\frac{b_0}{b_1^2}}\right)}{2} \tag{2.9}$$

The DC gain of $H(z)$ can be acquired by plugging $z = 1$ into (2.8):

$$H_0 = \frac{a_1}{1 + b_1 + b_0} \tag{2.10}$$

Since we want H_0 to be unity we have found another requirement for $H(z)$. By taking all the requirements into account we obtain a system of three equations in three unknowns, namely a_1, b_0 and b_1:

$$e^{-\frac{\omega_p T\left(1\pm\sqrt{1-4Q_i^2}\right)}{2Q_i}} = -\frac{b_1\left(1 \pm \sqrt{1 - 4\frac{b_0}{b_1^2}}\right)}{2} \tag{2.11}$$

$$\frac{a_1}{1 + b_1 + b_0} = 1 \tag{2.12}$$

Note that (2.11) actually consists of two equations. By solving these three equations for the unknowns a_1, b_0 and b_1 we get

$$a_1 = 1 - e^{-\frac{\omega_p T\left(1+\sqrt{1-4Q_i^2}\right)}{2Q_i}} - e^{-\frac{\omega_p T\left(1-\sqrt{1-4Q_i^2}\right)}{2Q_i}} + e^{-\frac{\omega_p T}{Q_i}} \tag{2.13}$$

$$b_0 = e^{-\frac{\omega_p T}{Q_i}} \tag{2.14}$$

$$b_1 = -e^{-\frac{\omega_p T\left(1+\sqrt{1-4Q_i^2}\right)}{2Q_i}} - e^{-\frac{\omega_p T\left(1-\sqrt{1-4Q_i^2}\right)}{2Q_i}} \tag{2.15}$$

for the coefficients which are all function of the cut-off frequency ω_p, the quality factor Q_i and the sampling interval T. By plugging in the previously specified values for the 6th order Butterworth lowpass filter we obtain the values in Table 2.2 as coefficients for the three second-order sections.

i	a_1	b_0	b_1
1	0.07338	0.54501	-1.47164
2	0.07903	0.64129	-1.56225
3	0.09034	0.84993	-1.75959

Table 2.2: z-domain coefficients for a 6th order Butterworth lowpass filter

Chapter 3

The SC Lowpass Filter

Once the coefficients for the general z-domain transfer function are found a topology for its hardware implementation has to be chosen. The SC biquad

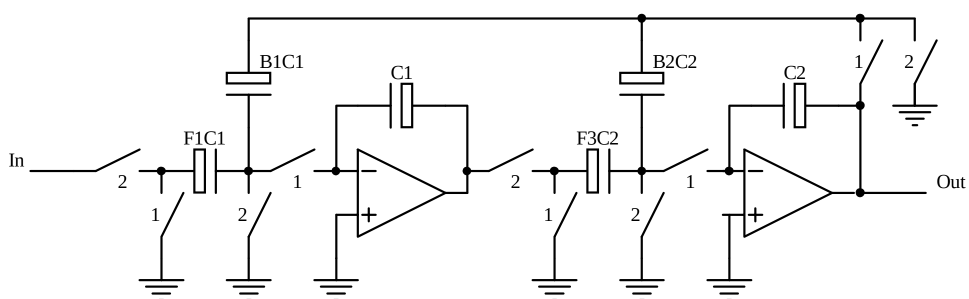

Figure 3.1: SC biquad realizing a second-order lowpass function.

circuit [2] that realizes a second-order lowpass function is depicted in Figure 3.1. The exact z-domain transfer function of this circuit is

$$H(z) = \frac{F_1 F_3 z^{-1}}{(1 + B_2)\, z^{-2} + (B_1 F_3 - B_2 - 2)\, z^{-1} + 1} \tag{3.1}$$

3.1 Finding the coefficients

By equating the coefficients of like powers with the coefficients in (2.8), we obtain the following equations:

$$a_1 = \frac{F_1 F_3}{1 + B_2}$$

$$
\begin{aligned}
b_0 &= \frac{B_1 F_3 - B_2 - 2}{1 + B_2} \\
b_1 &= \frac{1}{1 + B_2}
\end{aligned} \tag{3.2}
$$

This system contains four unknowns in only three equations. Consequently, there exists one free parameter, which is generally used to equalize the maximum voltage swing of the two amplifiers to achieve a maximum dynamic range. This is accomplished when the inputs of both integrators are completely balanced. In practice, it suffices to select $B_1 = F_3$. By introducing this additional equation and solving for the unknowns, namely B_1, F_1, B_2 and F_3, we obtain:

$$
\begin{aligned}
B_1 &= \frac{\sqrt{b_0\,(1 + b_0 + b_1)}}{b_0} \\
F_1 &= \frac{a_1}{\sqrt{b_0\,(1 + b_0 + b_1)}} \\
B_2 &= \frac{1 - b_0}{b_0} \\
F_3 &= \frac{\sqrt{b_0\,(1 + b_0 + b_1)}}{b_0}
\end{aligned} \tag{3.3}
$$

By plugging in the previously calculated values for a_1, b_0 and b_1 we obtain the values in Table 3.1 as SC biquad coefficients for the three second-order sections.

i	B_1	F_1	B_2	F_3
1	0.3669	0.3669	0.8348	0.3669
2	0.3511	0.3511	0.5594	0.3511
3	0.3260	0.3260	0.1766	0.3260

Table 3.1: SC biquad coefficients for a 6th order Butterworth lowpass filter

3.2 Design Verification

To verify the unity gain requirement for DC signals we plug in $z = 1$ into (3.1). By doing so we obtain:

$$H_0 = \frac{F_1}{B_1} \tag{3.4}$$

As we can see in Table 3.1 B_1 and F_1 are equal for each biquad. Thus, the DC gain is unity for all the sections i.e. the overall DC gain of the 6th order system is unity.

A behavioral simulation of the circuit can be achieved by finding the difference equation for each biquad.

$$out[n+2] = -b_1 out[n+1] - b_0 out[0] + a_1[n+1] \tag{3.5}$$

(3.5) shows the difference equation for one biquad found by taking the inverse z-transform of (2.8). After plugging in the values listed in Table 2.2 and

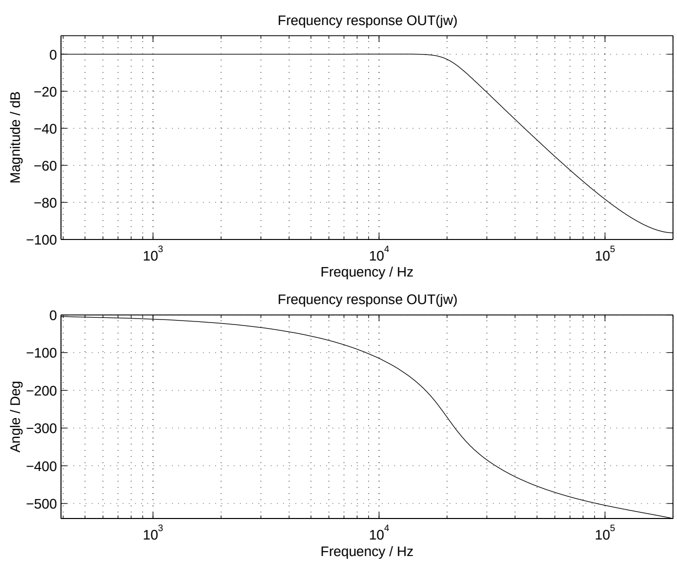

Figure 3.2: Frequency response of the 6th order filter.

cascading the three biquads the frequency response, shown in Figure 3.2 can be obtained by simulating the impulse response and taking its FFT.

3.3 Finding the Capacitor Sizes

As the last step of the theoretical design process the values for all the capacitors in the circuit have to be determined in a way, such that it can be physically implemented. This is done by making sure that the smallest capacitors in the circuit are unit capacitors. The physical measurement of such a unit capacitor is dependent on the semiconductor process used to implement the circuit. Doing so results in the values listed in Table 3.2.

i	C_1	B_1C_1	F_1C_1	C_2	B_2C_2	F_3C_2
1	2.7253	1	1	2.7253	2.2751	1
2	2.8485	1	1	2.8485	1.5934	1
3	3.0673	1	1	5.6635	1	1.8464

Table 3.2: Capacitor sizes

Chapter 4

VLSI Implementation

4.1 Building Blocks

4.1.1 Clock Generator

For a proper function of the SC circuit we do not only need a stable and symmetric system clock but also a non-overlapping two-phase clock derived from the system clock. For this purpose we use a two-phase clock generator which is depicted in Figure 4.1. This circuit guarantees the signals P1/NP1

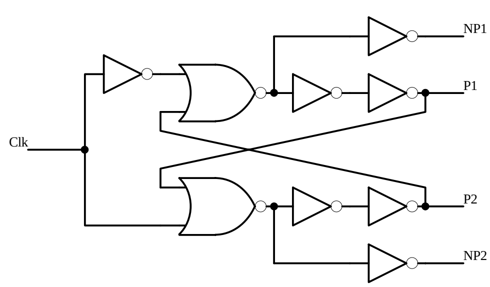

Figure 4.1: Schematic of the two-phase clock generator.

for the first phase and the signals P2/NP2 for the second phase to be non-overlapping, as depicted in timing diagram in Figure 4.2.

Since the output signals of the two-phase clock generator will be used by many other building blocks it is beneficial to create a bus structure. The layout in Figure 4.3 implements the circuit in a very compact and modular

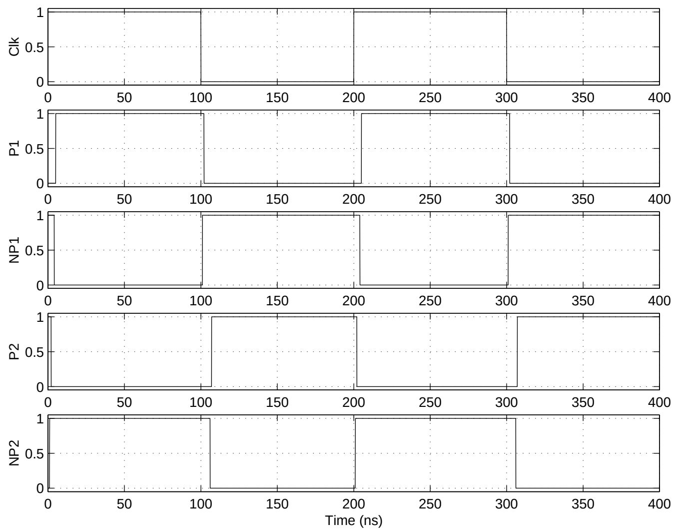

Figure 4.2: Timing diagram of the two-phase clock generator.

way that offers the possibility of using parallel bus lines and power rails for additional digital circuitry.

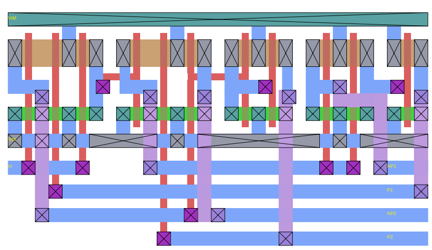

Figure 4.3: Layout of the two-phase clock generator.

4.1.2 Switches

The switches in a SC circuit are usually realized as a transmission gate, using a complementary CMOS device pair which is controlled by complementary gate signals. Each of the biquads uses 10 switches, and they are used in the exact same manner in all the sections, as depicted in Figure 4.4. Because

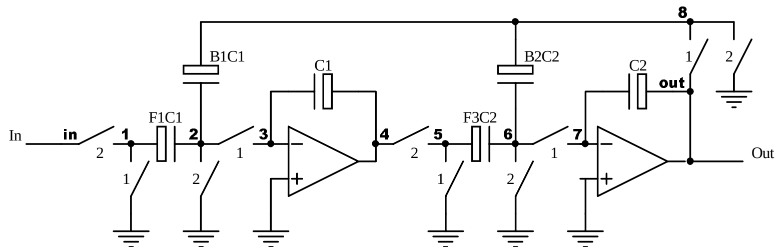

Figure 4.4: SC biquad realizing a second-order lowpass function.

of that it is possible to build a universal building block containing all the switches used for one second order section, as shown in Figure 4.5. One entity of this switch-box can then be used for each biquad.

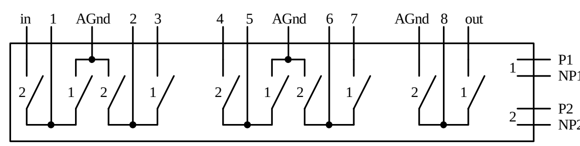

Figure 4.5: Universal switch-box for SC lowpass biquads.

The switches are controlled by the signals produced by the two-phase clock generator discussed in Section 4.1.1. Thus, when laying out the switch-box we have to make sure that we use the same bus and power rail structure used in the layout of the clock generator.

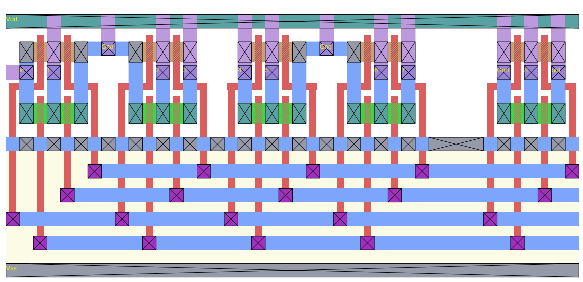

Figure 4.6: Layout of the switch-box.

4.1.3 Operational Amplifiers

The operational amplifiers play a very important role in SC circuits. Depending on the application there are high requirements for power supply rejection, phase margin, open loop gain, and slew rate. Hence, it is important to choose a topology that suits the purpose of the SC circuit. For this particular application a CMOS operational transconductance amplifier (OTA) was chosen, which is depicted in Figure 4.7. The CMOS devices M13, M14 and M15 form

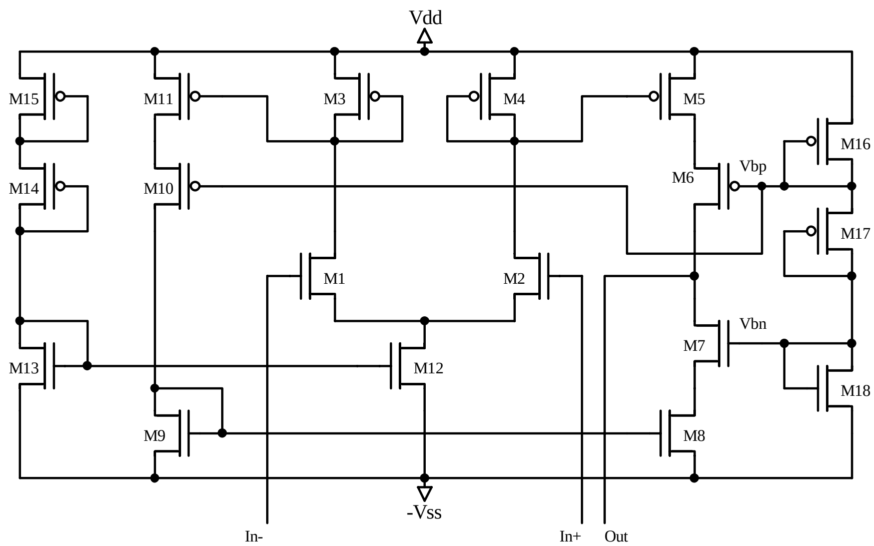

Figure 4.7: Schematic of the transconductance amplifier.

a cascode current source, which mirrors its constant current into the differential input stage via M12. The class AB (push-pull) output stage composed by M5, M6, M7 and M8 are biased by the two bias voltages V_{b_p} and V_{b_n} produced by the branch formed by M16, M17 and M18. A major advantage of this circuit is, that it does not need to be compensated by an internal capacitor. Thus, the phase margin of this type of amplifier only depends on the capacitive load at the output.

The layout of the transconductance amplifier is depicted in Figure 4.8. Note, that in order to keep the cell as small as possible the large transistors M5, M6, M7 and M8 have each been laid out as two parallel devices with half the channel width.

Since for each biquad two of these amplifiers are needed, it is useful to

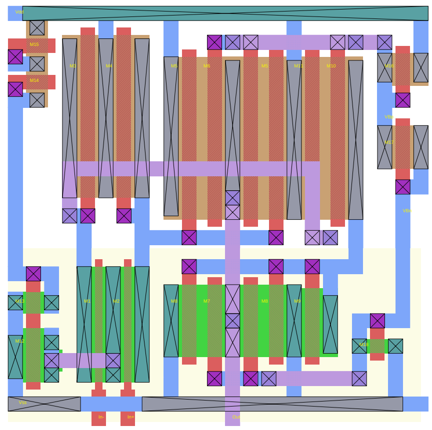

Figure 4.8: Layout of the transconductance amplifier.

combine them into one universal building block. Figure 4.9 shows an OTA that has been combined with a mirrored version of it. This way the biasing branch formed by M16, M17 and M18 can be shared by both amplifiers and therefore only has to be laid out once.

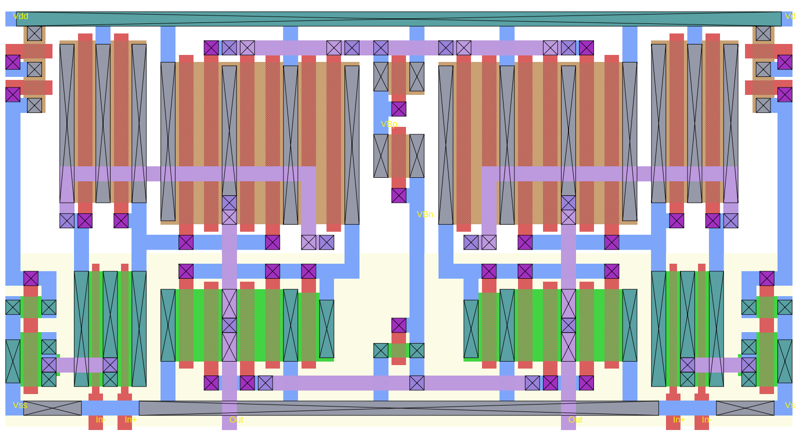

Figure 4.9: Layout of two combined OTA.

4.1.4 Capacitors

Before the entire circuit can be laid out the capacitor geometry for all the calculated sizes listed in Table 3.2 has to be determined. For capacitors of size 1 a unit capacitor is used, for non-integer values $R = 1..2$ the geometry can be calculated using the following formulas:

$$W \cong R\left(1 - \sqrt{1 - \frac{1}{R}}\right)$$
$$L \cong R\left(1 - \sqrt{1 + \frac{1}{R}}\right) \tag{4.1}$$

Capacitors with non-integer sizes that are greater than 2 have to be split into unit capacitors and one capacitor with a value within 1..2. Doing so guarantees optimal matching of the capacitors.

i	C_1	B_1C_1	F_1C_1	C_2	B_2C_2	F_3C_2
1	40×40	40×40	40×40	40×40	40×40	40×40
	24×114			24×114	27×75	
2	40×40	40×40	40×40	40×40	25×102	40×40
	24×124			24×124		
3	40×40	40×40	40×40	40×40	40×40	24×123
	40×40			40×40		
	32×53			40×40		
				40×40		
				25×108		

Table 4.1: Capacitor Geometry

In the next step we have to define the physical size of a unit capacitor. For optimal noise performance of the circuit we want the capacitors to be as large as possible since the thermal noise is reciprocal to the capacitor sizes. On the other hand, we want them to be as small as possible because the slew rate of each amplifier is inversely proportional to the capacitive load at the output. In our case we have to make sure that the biggest capacitor is smaller than 5pF which is the biggest capacity that the output stages of the OTA are capable of driving. Another requirement is the compactness of the layout. Depending on the priority of each requirement an optimal size of the unit capacitor has to be chosen. For our application we chose the unit capacitor to be 40λ wide. Note, that for the 1.2μm process used for this application λ corresponds to 0.6μm. Table 4.1 lists the physical sizes of the capacitors used for all three second order sections.

In the AMI 1.2μm semiconductor process, which is used to implement this circuit, the relative capacitance is specified to be $6 \cdot 10^{-4} \frac{\mathrm{F}}{\mathrm{m}^2}$. Therefore a λ^2 capacitor has the capacity $C_\lambda \cong 216 \cdot 10^{-18}$F. This leads to the capacities listed in Table 4.2.

i	C_1	B_1C_1	F_1C_1	C_2	B_2C_2	F_3C_2
1	0.94pF	0.35pF	0.35pF	0.94pF	0.79pF	0.35pF
2	0.98pF	0.35pF	0.35pF	0.98pF	0.55pF	0.35pF
3	1.06pF	0.35pF	0.35pF	1.96pF	0.35pF	0.64pF

Table 4.2: Capacitor Values

4.2 Layout

In a mixed signal environment it is crucial to separate the analog from the digital circuitry. In our system the analog part is represented by the three OTA pairs while the digital part consists of the two-phase clock generator and the three switch-boxes. These two parts are interfaced by the switched capacitors. Since the parasitic capacities between the capacitors and the substrate can not be neglected it is important that the substrate is not polluted by the digital circuitry. Consequently, the digital bus and the capacitor partition of the circuit have to be shielded by guard-rings and p-wells connected to digital V_{ss} and analog GND respectively. This leads to the finished layout depicted in Figure 4.10.

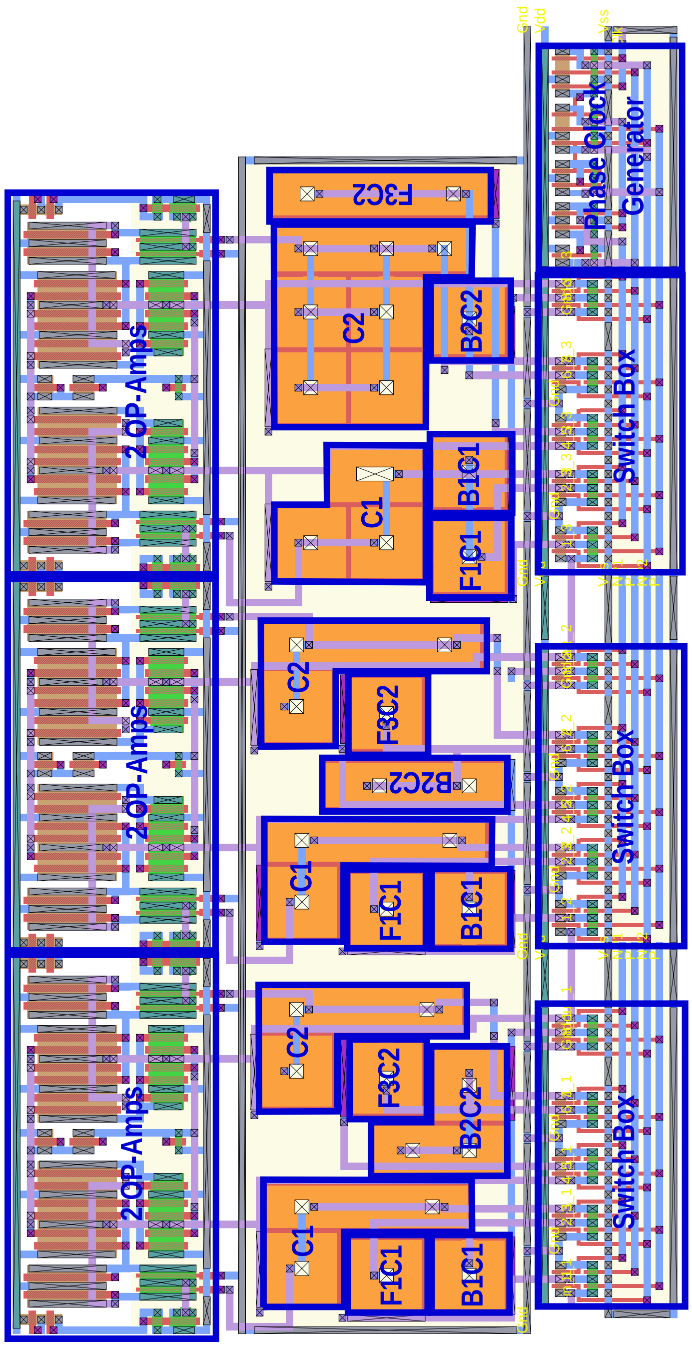

Figure 4.10: The finished layout of the 6th order SC Butterworth filter

Chapter 5

Conclusion

Once the circuit is laid out completely, the next logical step would be to extract the layout and simulate the hardware implementation using analog simulation software, e.g. H-Spice. The output of the simulator would have to be analyzed in order to be able to measure the circuits performance. If necessary, the layout would have to be fine tuned according to the results of the simulation.

Unfortunately, once the theoretical part of the project was completed, H-Spice was not available anymore due to license problems. Hence, the performance of the OTA, which were originally laid out for a 2μm process, could not be identified. Because of that, the necessary adjustments for the AMI 1.2μm process could not be made. It is very likely, that the amplifiers do not have a very high open-loop gain. This generally results in a shifting of the poles, which leads to a degradation of the filter performance.

The design and implementation of mixed signal circuits is a challenge for every design engineer, and it requires a skill that can not be learned by just taking classes and reading the necessary books. It is not 'textbook knowledge' that makes a good designer, but the experience which only can be obtained by practice and exposure to design projects.

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