Master Thesis Proposal

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A. Title of Study

Digital Decimating Filter For A Monolithic Sonar Receiver

B. Problem Statement

Synthesize a digital decimating filter for delta-sigma modulated input signals. Implement the design by programmable logic (e.g. Xilinx XC4000 series) in order to obtain a high level hardware based description of the system. Simulate and verify the filter performance.

C. Justification for and Significance of Study

A typical sonar system consists of a large sensor array followed by a digital beamformer that spatially analyzes the received data. In order to process the sensors' data values digitally, the signals are first converted into the digital domain. In the past, this work has been accomplished by off-the-shelf analog-to-digital converters with multi-bit outputs which subsequently have been fed into the digital beamformer. For systems with a higher number

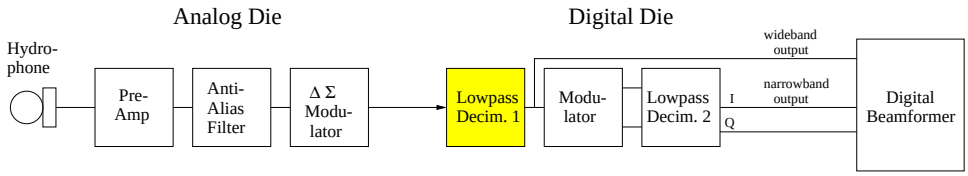

Figure 1: Monolithic Sonar Receiver.

of channels (more than about 50), issues like hardware cost, dimensionality, and electrical problems gain importance.

A more cost and space effective way of implementing the analog-to-digital conversion is to use delta-sigma modulators that are specially designed to acquire the sensors' output signals. The modulators' pulse density modulated (PDM) output comprises the oversampled input signals and wideband noise (off-band), which stems from the quantization process. In order to obtain wideband output signals, which can be further processed by either a beamformer or additional filters for narrowband beamforming, the delta-sigma modulator output signals have to be digitally low-pass filtered and decimated. Figure 1 shows one channel of such a system in form of a block diagram.

D. Methodology

In preparing for this research, several books and papers about delta-sigma modulation [1, 2] and digital filter design [3, 4] have been studied. As a next step, a digital FIR low pass filter has been designed using various MATLAB routines that have been written for this purpose. A supporting simulation using procedures out of the DelSi toolbox [5] presents its functionality and provides a performance measure. Once the performance was verified, a concept for implementing the decimating filter by field programmable gate array (FPGA) technology was developed and a hardware simulator for MATLAB was programmed. As a last step, the design was implemented by FPGA technology (i.e. XILINX XC4000 series), and a functional as well as a structural timing simulation was conducted to verify the systems performance. This work has been done between January 1999 and August 1999.

E. Resources Required

Resource:	Provided by:
Workstation	URI Electrical Engineering Department
Books/Technical reports	URI Library and Personal Funds
MATLAB Software	URI Electrical Engineering Department
XILINX Software	URI Electrical Engineering Department

F. References

[1] J. C. Candy and G. C. Temes, *Oversampling Methods for A/D and D/A Conversion*, pp. 1–33. IEEE Press, 1991.

[2] G. Fischer and A. J. Davis, "Delta-sigma modulation," in *Wiley Encyclopedia of Electrical and Electronics Engineering* (J. G. Webster, ed.), vol. 19, pp. 244–254, New York: John Wiley & Sons, Inc., 1999.

[3] A. V. Oppenheim and R. W. Schafer, *Digital Signal Processing*, ch. 5. Prentice-Hall, 1975.

[4] L. B. Jackson, *Digital Filters and Signal Processing*, ch. 8-13. Kluwer Academic Publishers, 1995.

[5] A. J. Davis and G. Fischer, "Delsi - A design and simulation tool for delta-sigma modulators," in *IMEKO* 2^{nd} *International Workshop on ADC Modeling and Testing*, (Tampere, Finland), pp. 213–218, 1-3 June 1997.